CALL FOR PAPERS

SPIE. ADVANCED LITHOGRAPHY+ PATTERNING

San Jose McEnery Convention Center
San Jose, California, United States

SUBMIT ABSTRACTS BY
11 SEPTEMBER 2024

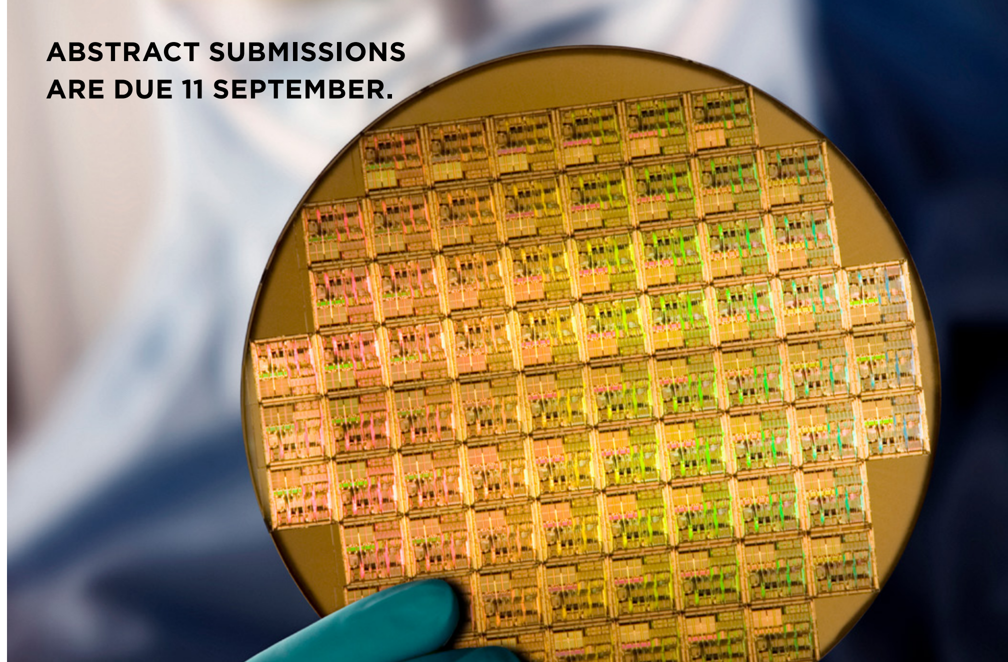
spie.org/alcall
#SPIElitho

ADVANCED LITHOGRAPHY+ PATTERNING

San Jose McEnery Convention Center
San Jose, California, United States

Conferences and Courses
23–27 February 2025

Exhibition
25–26 February 2025



Share your research and make important connections throughout the semiconductor industry

Stay up to date via Email

Sign up to receive email about SPIE Advanced Lithography + Patterning.

spie.org/signup

Contents

CONFERENCE AL101 2
Optical and EUV Nanolithography XXXVIII
Chairs: **Martin Burkhardt; Claire van Lare**

CONFERENCE AL102. 4
DTCO and Computational Patterning IV
Chairs: **Neal V. Lafferty; Harsha Grunes**

Conference AL103 6
Metrology, Inspection, and Process Control XXXIX
Chairs: **Matthew J. Sendelbach; Nivea G. Schuch**

CONFERENCE AL104 9
Novel Patterning Technologies 2025
Chairs: **Ricardo Ruiz; Richard A. Farrell**

CONFERENCE AL105 11
Advances in Patterning Materials and Processes XLII
Chairs: **Douglas Guerrero; Ryan Callahan**

CONFERENCE AL106 13
Advanced Etch Technology and Process Integration for Nanopatterning XIV
Chairs: **Nihar Mohanty; Efrain Altamirano-Sánchez**

Student opportunities 15
Submission of Abstracts 16
General Information 19

Plan to participate

SPIE Advanced Lithography + Patterning symposium has been the premier conference on lithography and patterning in the semiconductor industry since 1976. It offers a forum to exchange technical advances and to showcase products in semiconductor lithography, patterning and related technologies for the worldwide practitioners of semiconductor technology and manufacturing with a focus on industrial applications. SPIE Advanced Lithography + Patterning covers the entire value-chain in semiconductor lithography and patterning, including circuit design, materials, masks, lithography and etch tools, processes, computational lithography, metrology, testing and yield improvement as well as emerging fields of novel patterning, artificial intelligence (machine learning, deep learning), augmented reality and virtual reality (AR/VR), and sustainability.

The recent great global semiconductor chip shortage highlighted the essential role of the semiconductor industry to almost every aspect of the economy, human health, national security, and quality of life of billions of global citizens. Advanced semiconductor chips are also the foundation of new innovations such as generative artificial intelligence. The remarkable historic progress of packing more transistors per chip with ever decreasing cost per transistor has been fueled by continual technological advances in lithography and patterning. These technological advances have been made possible by the ingenuity, dedication and hard work of engineers and scientists around the world. They are also a testament of the unparalleled open global collaborations throughout the entire ecosystem in the semiconductor industry. SPIE Advanced Lithography and Patterning aims to provide a venue to enable such open and inclusive global collaborations and to provide a platform to facilitate product showcase, business engagements and professional networking in semiconductor lithography, patterning and related technologies.

SPIE Advanced Lithography + Patterning 2025 will cover the full spectrum of challenges and advances in the state-of-the-art lithography and patterning technology through six topical conferences. Advances in semiconductor nano- and micro-patterning will be addressed in sessions covering optical lithography, extreme ultraviolet (EUV) lithography, computational patterning, metrology/inspection, patterning materials, etch/films/deposition technology, and System-Design-Technology co-optimization. As novel patterning and other related technologies, such as 3D heterogenous integration, IoT devices such as MEMS and sensors, AR/VR devices, flat-panel displays, have become more widely explored, related topics in these areas will also be addressed.

SPIE Advanced Lithography + Patterning consists of six distinct conferences. They are organized by experts and current practitioners of the art in their respective fields.

Joint sessions between the conferences will be included along with five (5) predefined tropical tracks: (1) artificial intelligence and machine learning (AI/ML), (2) stochastics, (3) Edge Placement Error (EPE) /overlay, (4) advanced packaging, and (5) sustainability. These topical tracks will offer attendees the opportunity to cover important common topics across different conferences and to minimize presentation overlap.

In addition to the six (6) conferences, SPIE Advanced Lithography + Patterning 2025 will offer symposium plenary session(s) where executives, innovators and thought leaders will share grand challenges, major inflection points, industry trends and technology roadmaps. It will also host panel sessions where movers and shakers in the field will discuss and debate important topics of interest to the lithography and patterning community in particular and the semiconductor industry in general.

Moreover, SPIE Advanced Lithography + Patterning 2025 will offer a series of short courses developed and taught by some of the most respected experts in the field provide an excellent forum for newcomers to the field as well as seasoned experts looking to expand their knowledge base. Details of these short courses and other topics can be found online closer to the time of the symposium.

We welcome your contribution to and participation in SPIE Advanced Lithography + Patterning and urge you to submit abstracts to the appropriate conferences as described in the individual calls for papers and encourage your colleagues to do the same.

SPIE Advanced Lithography + Patterning recognizes the importance of fostering new generations of innovative and strongly skilled lithographers and patterning engineers for the development of electronic and photonic devices and systems technology to advance the digital age. We have developed and will continue a student grant program to attract students to contribute to and to attend SPIE Advanced Lithography + Patterning. We also established a student mentoring program to connect industry technology leaders with students to guide the students in exploring and planning to succeed in the semiconductor industry. We would like to encourage students to participate in this exciting and rewarding program.

We welcome you to contribute, to connect, to learn, to grow and to prosper together through SPIE Advanced Lithography and Patterning.

SYMPOSIUM CHAIR:

Qinghuang Lin
LinkTech International (United States)

SYMPOSIUM CO-CHAIR:

John Robinson
KLA (United States)

Optical and EUV Nanolithography XXXVIII (AL101)

Conference Chair: **Martin Burkhardt,** IBM Thomas J. Watson Research Ctr. (United States)

Conference Co-Chair: **Claire van Lare,** ASML Netherlands B.V. (Netherlands)

Program Committee: **Christopher Neil Anderson,** xLight, Inc. (United States); **Steven L. Carson,** Intel Corp. (United States); **Will Conley,** Cymer, LLC (United States); **Huixiong Dai,** Applied Materials, Inc. (United States); **Andreas Erdmann,** Fraunhofer-Institut für Integrierte Systeme und Bauelementetechnologie IISB (Germany); **Allen H. Gabor,** IBM Thomas J. Watson Research Ctr. (United States); **Andreas Greiner,** Infineon Technologies Dresden GmbH (Germany); **Naoya Hayashi,** Dai Nippon Printing Co., Ltd. (Japan); **Soichi Inoue,** KIOXIA Corp. (Japan); **Chan-Uk Jeon,** Toppan Photomask Co., Ltd (United States); **Young Seog Kang,** SAMSUNG Electronics Co., Ltd. (Republic of Korea); **Bryan S. Kasprowicz,** HOYA Corp. USA (United States); **Insung Kim,** SAMSUNG Electronics Co., Ltd. (Republic of Korea); **Ted Liang,** Intel Corp. (United States); **Chang-Moon Lim,** SK Hynix, Inc. (Republic of Korea); **Luciana Meli,** IBM Thomas J. Watson Research Ctr. (United States); **Lawrence S. Melvin III,** Synopsys, Inc. (United States); **Iacopo Mochi,** Paul Scherrer Institut (Switzerland); **Ken-Ichiro Mori,** Canon Inc. (Japan); **Patrick P. Naulleau,** EUV Technology (United States); **Jens Timo Neumann,** Carl Zeiss SMT GmbH (Germany); **Vicky Philipsen,** imec (Belgium); **Moshe E. Preil,** Carl Zeiss AG (United States); **Paulina A. Rincon-Delgadillo,** imec (Belgium); **Katrina Rook,** Veeco Instruments Inc. (United States); **Bruce W. Smith,** Rochester Institute of Technology (United States); **Martin Y. Sohn,** National Institute of Standards and Technology (United States); **Regina Soufli,** Consultant (United States); **Akiyoshi Suzuki,** AS Lithography Consulting (Japan); **Edita Tejnil,** Siemens EDA (United States); **Geert Vandenberghe,** imec (Belgium); **Yoji Watanabe,** Nikon Corp. (Japan); **Obert R. Wood II,** Retired (United States); **Kenji Yamazoe,** TSMC North America (United States)

EXTENDED ABSTRACT REQUEST

An optional PDF file is requested in step 7 of the abstract submission process:

- 2-page maximum extended abstract. The extended abstract must be submitted as a separate PDF document limited to two pages, including tables and figures. Include author names and affiliations; text; any figures; tables, or images; and sufficient data for committee review.

Extended abstracts will be used only for the purpose of review and will not be published.

For over 50 years photolithography has been at the center of the growth for the semiconductor industry, enabling the progress of Moore's law. The art of shaping matter with photons influences the way we live today and will continue to do so in the future. A large part of this progress has been documented in the proceedings of this conference that was incepted in 1988 as "Optical/Laser Microlithography", and merged with the EUV Lithography conference in 2022.

The Optical and EUV Nanolithography XXXVIII conference covers EUV and Optical projection-based lithography systems, practices, and their applications in IC technology. It is the leading forum for scientists and engineers from around the world to present and discuss research on the advancement of lithography technologies.

Please note that all authors are expected to submit manuscripts for the conference proceedings, as is the case in all SPIE conferences. We welcome technical and scientific papers in the following areas:

LITHOGRAPHY EQUIPMENT

- optical and EUV lithography equipment
- steppers, scanners, and mask-less exposure tools
- high resolution (high NA) and high depth of focus (low NA) exposure systems, including for non-IC applications (IoT, heterogenous integration)
- investigations on productivity, imaging and overlay performance and control, including aberrations, flare, and out-of-band radiation

SOURCES

- light sources and source characterization for EUV and optical lithography systems
- optical and EUV sources, including efficiency, cleaning, reliability, and sustainability

MASKS

- optical and EUV mask substrates and blanks, including absorber materials and patterning
- patterned and blank mask inspection using actinic, e-beam, or DUV methods
- defect and roughness characterization, mitigation, and repair
- pellicle development and platform integration
- mask writing tools and techniques

PATTERNING

- optical system and mask induced defect, electrical, and yield signatures
- resolution enhancement techniques
- imaging simulations and source-mask optimization (SMO)
- tool-to-tool mixing and matching and overlay control, including mid-UV to DUV to EUV full field, half field, and multiple fields
- process optimization and stochastics control, including novel photoresist and underlayer applications

ASML BEST STUDENT PAPER

Students submitting papers to Optical and EUV Nanolithography XXXVII will be considered for the ASML Best Student Paper. This award is given each year at this conference and recognizes extraordinary work achieved by students interested in the photolithography field, and strongly supports the contributions made to scientific advancement at the conference. The award includes a plaque along with a monetary award to help the student's future research activities. Students are also encouraged to apply for travel grants to attend the conference and for the Nick Cobb Memorial Scholarship.

Submit your abstract today: **www.spie.org/alcall**

DTCO and Computational Patterning IV (AL102)

Conference Chair: **Neal V. Lafferty,** Siemens EDA (United States)

Conference Co-Chair: **Harsha Grunes,** Intel Corp. (United States)

Program Committee: **Jason P. Cain,** Advanced Micro Devices, Inc. (United States); **Luigi Capodieci,** Motivo, Inc. (United States); **Lifu Chang,** MOSIS Integrated Circuit Fabrication Service (United States); **Dan J. Dechene,** IBM Thomas J. Watson Research Ctr. (United States); **David M. Fried,** Lam Research Corp. (United States); **Yuri Granik,** Siemens EDA (United States); **Srividya Jayaram,** Siemens EDA (United States); **Seongtae Jeong,** SAMSUNG Electronics Co., Ltd. (Republic of Korea); **Ryoung-Han Kim,** imec (Belgium); **Sachiko Kobayashi,** KIOXIA Corp. (Japan); **Kafai Lai,** The Univ. of Hong Kong (Hong Kong, China); **Ya-Chieh Lai,** Cadence Design Systems, Inc. (United States); **Lars W. Liebmann,** Intel Corp. (United States); **Kevin Lucas,** Synopsys, Inc. (United States); **Lawrence S. Melvin III,** Synopsys, Inc. (United States); **Shigeki Nojima,** KIOXIA Corp. (Japan); **David Z. Pan,** The Univ. of Texas at Austin (United States); **Piyush Pathak,** Cadence Design Systems, Inc. (United States); **Michael L. Rieger,** Consultant (United States); **Vivek K. Singh,** NVIDIA Corp. (United States); **Chun-Ming Wang,** Western Digital Corp. (United States); **Lynn T. Wang,** GlobalFoundries (United States); **Yayi Wei,** Institute of Microelectronics, Chinese Academy of Sciences (China); **Chi-Min Yuan,** NXP Semiconductors (United States)

EXTENDED ABSTRACT REQUEST

An optional PDF file is requested in step 7 of the abstract submission process:

- 2-page maximum extended abstract. The extended abstract must be submitted as a separate PDF document limited to two pages, including tables and figures. Include author names and affiliations; text; any figures; tables, or images; and sufficient data for committee review.

Extended abstracts will be used only for the purpose of review and will not be published.

The 2025 Design Technology Co-Optimization (DTCO) and Computational Patterning conference at SPIE Advanced Lithography and Patterning is calling for papers. Topics including computational patterning, design technology co-optimization (DTCO), system technology co-optimization (STCO), design for manufacturability (DFM), design for yield (DFY), deep learning and machine learning, and modeling to co-optimize design and technology to improve chip power, performance, area, and cost are encouraged as focus. In addition, academic topics potentially relevant to the semiconductor industry are encouraged to submit. Authors agree to the requirement of a manuscript submission, minimum 2-page, before the conference. Topics of interest include, but are not limited to:

DESIGN TECHNOLOGY CO-OPTIMIZATION (DTCO) AND SYSTEM TECHNOLOGY CO-OPTIMIZATION (STCO)

- pattern-based design optimization
  - design-intent to manufacturing
  - performance-power-manufacturability optimization
  - layout style and lithography co-optimization (including optical source and design co-optimization)
  - design for novel patterning process
- design optimization for technology
  - DTCO for standard cells and memory including standard cell, SRAM, and digital designs
  - DTCO for device, Integration, and tools
- STCO and 3D integration
  - 3D packaging, integration and heterogeneous integration and its impact to design, DFM, OPC and other fields.

DESIGN FOR MANUFACTURING (DFM), DESIGN FOR YIELD (DFY): TECHNOLOGY, IP AND SYSTEM

- physical layout optimization
  - design-rule development strategies and methodologies
  - layout optimization for systematic and random yield loss reduction
  - layout optimization for minimizing circuit variability
- design and verification methodologies including hot spot analysis
- manufacturing friendly circuit design styles and methodologies
- design-to-manufacturing methodologies for analog circuits, MEMS, and other microlithography applications
- design-to-manufacturing economics
  - cost-performance tradeoffs between design and manufacturing
  - design-to-manufacturing flow methodologies for productivity improvement, time-to-market, and cost reduction
- DFM for “more than Moore” applications (analog, RF, digital/SoC, etc.).

COMPUTATIONAL PATTERNING (EUV AND DUV)

- computational patterning consideration for anamorphic high-NA EUV, including stitching impacts on design and DTCO applications for mitigation
- new approaches for multi-patterning, decomposition, and interaction with design and patterning
- propagating electrical design intent for RET/OPC and manufacturing optimization and verification.

DEEP LEARNING, MACHINE LEARNING, AND AI TECHNIQUES

- machine learning on design, process, mask, and OPC methodologies
- new machine learning concepts and algorithms that are potentially applicable to semiconductor industry
- data analytics for layout analysis and optimization or process modeling and control.

MODELING, SIMULATION, AND COMPUTATION

- modeling for accuracy and defect detection
- computational acceleration through GPU, efficient algorithms, etc.
- applications of new computation architectures such as quantum computing, TPU, etc.

Students planning to attend the conference encouraged to apply for travel grants to attend the conference and for the Nick Cobb Memorial Scholarship.

Submit your abstract today: **www.spie.org/alcall**

Metrology, Inspection, and Process Control XXXIX (AL103)

Conference Chair: **Matthew J. Sendelbach,** TEL Technology Ctr., America, LLC (United States)

Conference Co-Chair: **Nivea G. Schuch,** Applied Materials (France)

Program Committee: **Ofer Adan,** Applied Materials Israel, Ltd. (Israel); **John A. Allgair,** BRIDG (United States); **Masafumi Asano,** Tokyo Electron Ltd. (Japan); **Bryan M. Barnes,** National Institute of Standards and Technology (United States); **Cornel Bozdog,** Onto Innovation Inc. (United States); **Benjamin D. Bunday,** AMAG nanometro (United States); **Xiaomeng Chen,** Taiwan Semiconductor Manufacturing Co. Ltd. (Taiwan); **Hugo Cramer,** ASML Netherlands B.V. (Netherlands); **Timothy F. Crimmins,** Intel Corp. (United States); **R. Joseph Kline,** National Institute of Standards and Technology (United States); **Shunsuke Koshihara,** Hitachi High-Tech Corp. (Japan); **Yi-sha Ku,** Industrial Technology Research Institute (Taiwan); **Byoung-Ho Lee,** Hitachi High-Technologies Corp. (Japan); **Myungjun Lee,** SAMSUNG Electronics Co., Ltd. (Republic of Korea); **Philippe Leray,** imec (Belgium); **Narender Rana,** KLA Corp. (United States); **Christopher J. Raymond,** Onto Innovation Inc. (United States); **John C. Robinson,** KLA Corp. (United States); **Daniel Schmidt,** IBM Thomas J. Watson Research Ctr. (United States); **Younghoon Sohn,** SAMSUNG Electronics Co., Ltd. (Republic of Korea); **Alexander Starikov,** I&I Consulting (United States); **Alok Vaid,** GlobalFoundries (United States)

EXTENDED ABSTRACT REQUEST

An optional PDF file is requested in step 7 of the abstract submission process:

- 2-page maximum extended abstract. The extended abstract must be submitted as a separate PDF document limited to two pages, including tables and figures. Include author names and affiliations; text; any figures; tables, or images; and sufficient data for committee review.

Extended abstracts will be used only for the purpose of review and will not be published.

Detection, analysis, identification, and control of error sources and defects in semiconductor device research, development, and manufacturing continue to enable rapid improvements throughout the industry, from equipment monitoring and control to wafer processing and packaging. Long gone, however, are the days when nearly every type of semiconductor manufacturing metrology fell into one of three categories: CD, overlay, and film thickness. Now, applications that once were obscure are becoming mainstream and crucial, such as stochastics and contour metrology. Techniques—many for measuring intrinsic properties of device materials—that were traditionally considered incompatible with, or economically not justifiable for, high volume manufacturing have since become essential in the fab.

Still fundamental to reducing manufacturing costs, defect inspection of masks and wafers guides the path to higher fab yields. Development of materials, equipment, and processing in lithography, etch, and other areas drives further innovation of metrology tools and applications. And continued advancements in machine learning, data analytics, modeling, and hybrid metrology further extend the capabilities of metrology and inspection while providing valuable process and device insight, enhancing process control, and improving fab efficiency.

This conference is the leading forum for the exchange of foundational information on, and the discussion of, novel concepts in patterning-related metrology, inspection, and process control in semiconductor research, development, and manufacturing. Industrial, governmental, research, and academic organizations (including students) are encouraged to submit original technical papers in these and related technology areas listed below.

NOTE: Commercialism within submissions, presentations, and manuscripts is strongly discouraged, reduces the chance of earning oral presentation status, and may result in the rejection of the submission or the prevention of the presentation and/or manuscript from being published.

METROLOGY AND INSPECTION TECHNIQUES

- optical (EUV-UV-visible-IR) and X-ray full-field and scanned microscopy, interference microscopy, and scatterometry
- particle-beam scanned microscopy, including CD-SEM, XSEM, and TEM
- cantilever-based scanning probe microscopy, including AFM
- acoustic/phonon-based metrology
- parametric electrical testing and other device performance-based metrology
- defect inspection and review techniques based on optics (including X-rays), electron and other particle beams, and cantilever-based scanning probes
- lab and physical characterization techniques
- novel or emerging metrology and inspection methods and solutions.

APPLICATIONS IN CRITICAL DIMENSION, PATTERN PLACEMENT, AND OVERLAY

- 1D, 2D, and 3D metrology of pattern pitch, width, and placement, including within-device layouts
- alignment, registration, and overlay metrology
- optical, CD-SEM, and AFM based in-die overlay on small targets and devices
- contour metrology, and metrology of the feature edge, edge profile, and edge position
- design-based metrology, including distance-to-design
- stochastics, including roughness of edge, width, and centerline
- Edge Placement Error (EPE).

APPLICATIONS IN DEFECT DETECTION, CHARACTERIZATION, ANALYSIS, AND CONTROL

- defect inspection and review of, and defect reduction on, wafers and photomasks
- detection and control of systematic, random, and low-photon-count stochastic pattern defects
- yield improvement related to defect reduction
- high resolution and high throughput inspection, including methods that use fast electron beams, multi-beams, and backscattered electron (BSE) detection
- artificial intelligence and machine learning applied to defect detection, analysis, and control
- design-based inspection
- environmental contamination, including impacts on processing and defects.

APPLICATIONS IN PROCESS DEVELOPMENT, CHARACTERIZATION, CONTROL, PERFORMANCE, AND YIELD

- metrology to support the development of lithography, etch, and other patterning-related processes
- process metrology and monitors, segmentation, and reduction of variance
- metrology sampling, excursion detection, costs, device performance, and yield
- design-based metrology
- metrology for design rules and process margins, budgeting, and budget control
- data analysis and visualization, modeling, and fingerprint detection
- advanced process control, data feedback and feed forward
- big data analysis and diagnostic methodologies, data management.

OTHER METROLOGY AND INSPECTION APPLICATIONS

- materials characterization, materials interfaces, composition metrology, and elemental analysis
- metrology for photomasks, including pre-compensation, Optical Proximity Correction (OPC), and phase-shifting
- novel or emerging metrology and inspection applications
- applications in emerging patterning technologies, including EUV lithography, direct write, nanoimprint, and Directed Self-Assembly (DSA)
- applications in 3D & Heterogeneous Integration (3D & HI), including advanced packaging, wafer geometry, wafer bonding, Through-Silicon Vias (TSVs), and Backside Power Delivery Networks (BSPDNs)
- applications in other micro- and nano-systems, including displays, thin-film heads, Microelectromechanical Systems (MEMS), Microoptoelectromechanical Systems (MOEMS), lab-on-a-chip, integrated optoelectronics, and quantum systems.

MEASUREMENT SYSTEM MODELING AND SIMULATION

- physics and mathematical models of metrology process and detection methods
- physical characterization of both systems and samples, model parameters
- virtual and computational metrology
- artificial intelligence and machine learning applied to metrology and inspection
- data analysis methods, library-based image analysis, and algorithms.

CALIBRATION AND ACCURACY

- metrology quality, error diagnostics, and data culling
- measurement resolution and error, including precision and accuracy
- standards and reference materials, calibration methods, hybrid metrology
- reference measurement systems and metrology comparisons
- tool fleet performance, maintenance, and matching.

PERFORMANCE LIMITS AND SUSTAINABILITY

- responses to commanded skews and across-technology comparisons
- models of tool-sample interaction, noise, and error mechanisms
- sustainability related to or impacted by metrology, inspection, or process control.

THE DIANA NYYSSONEN MEMORIAL BEST PAPER AWARD

The Diana Nyyssonen Memorial Best Paper Award for the best paper of the Conference on Metrology, Inspection, and Process Control recognizes the most significant current contribution to the field, based on the technical merit and persuasiveness of the oral presentation, as well as on the overall quality of the manuscript published in the conference proceedings. Presented at the subsequent year's conference, the Diana Nyyssonen Memorial Best Paper Award consists of an SPIE citation and an honorarium.

AWARD SPONSORED BY

HITACHI
Inspire the Next
Hitachi High-Tech

Submit your abstract today: **www.spie.org/alcall**

Metrology, Inspection, and Process Control XXXIX (AL103) continued

THE KAREL URBÁNEK BEST STUDENT PAPER AWARD

The Karel Urbánek Best Student Paper Award recognizes the most promising contribution to the field by a student, based on the technical merit and persuasiveness of the paper presented at the current year's conference. Awarded near the end of the week, the Karel Urbánek Best Student Paper Award consists of an SPIE citation and an honorarium.

To be eligible, the leading author and presenter of the paper must be a student. To establish eligibility, the bio submitted with the abstract must state the student's academic status and institution, as well as their advisor's name and contact information.

AWARD SPONSORED BY

Students are encouraged to apply for travel grants to attend the conference and for the Nick Cobb Memorial Scholarship.

THE VLADIMIR UKRAINTSEV AWARD FOR COLLABORATIONS IN METROLOGY

The Vladimir Ukraintsev Award for Collaborations in Metrology recognizes the most significant publication on inter-disciplinary explorations of metrology accuracy, round-robin studies, dissemination of best-known methods, and other industry collaborations. The recipient will be determined by the Metrology, Inspection, and Process Control program committee on occasion, as warranted, based on the publication's potential to influence the industry via an oral or poster presentation, as well as on the overall quality of the manuscript published in the conference proceedings. The Vladimir Ukraintsev Award for Collaborations in Metrology, when awarded, will be presented at the subsequent year's conference, and consists of an SPIE citation and an honorarium.

Submit your abstract today: **www.spie.org/alcall**

Novel Patterning Technologies 2025 (AL104)

Conference Chair: **Ricardo Ruiz,** Lawrence Berkeley National Lab. (United States)

Conference Co-Chair: **Richard A. Farrell,** Meta (United States)

Program Committee: **Alan D. Brodie,** KLA Corp. (United States); **Tito L. Busani,** The Univ. of New Mexico (United States); **Emine Cagin,** Heidelberg Instruments Nano AG (Switzerland); **Sandip Halder,** SCREEN SPE Germany GmbH (Germany); **Naoya Hayashi,** Dai Nippon Printing Co., Ltd. (Japan); **Daniel J. C. Herr,** The Univ. of North Carolina at Greensboro (United States); **Tatsuhiko Higashiki,** KIOXIA Corp. (Japan); **Koji Ichimura,** Dai Nippon Printing Co., Ltd. (Japan); **Takuya Kono,** KIOXIA Corp. (Japan); **Stephen M. Kuebler,** Univ. of Central Florida (United States); **J. Alexander Liddle,** National Institute of Standards and Technology (United States); **Chi-Chun Liu,** IBM Thomas J. Watson Research Ctr. (United States); **Hans Loeschner,** IMS Nanofabrication GmbH (Austria); **Laurent Pain,** CEA-LETI (France); **Eric M. Panning,** SiClarity Inc. (United States); **Ivo W. Rangelow,** Technische Univ. Ilmenau (Germany); **Douglas J. Resnick,** Canon Nanotechnologies, Inc. (United States); **Martha I. Sanchez; Chandrasekhar Sarma,** Wolfspeed, Inc. (United States); **Gurpreet Singh,** Intel Corp. (United States); **Lovejeet Singh,** JSR Micro, Inc. (United States); **Ines A. Stolberg,** Vistec Electron Beam GmbH (Germany); **Mark A. van de Kerkhof,** ASML Netherlands B.V. (Netherlands); **Niels Wijnaendts vam Resandt,** Lab14 (United States)

EXTENDED ABSTRACT REQUEST

An optional PDF file is requested in step 7 of the abstract submission process:

- 2-page maximum extended abstract. The extended abstract must be submitted as a separate PDF document limited to two pages, including tables and figures. Include author names and affiliations; text; any figures; tables, or images; and sufficient data for committee review.

Extended abstracts will be used only for the purpose of review and will not be published.

The Novel Patterning Technologies conference serves as a platform for addressing current and future challenges in patterning technologies, critical to extend scaling, complement existing approaches, address sustainability challenges and enable functional patterning for emerging and convergent applications, including More Moore and More-than-Moore domains. Bringing together a diverse cohort of industry and academia leaders, this conference facilitates the exchange of expertise within and beyond the semiconductor sphere.

<p>Showcasing cutting-edge lithography and patterning innovations, this conference addresses the needs of both mature and leading-edge semiconductor IC nodes, wafer-level packaging, heterogeneous integration, power electronics, and autonomous or AI-driven manufacturing. Additionally, it also explores applications in non-Si and non-IC fields, such as healthcare, communications, and energy technologies. Featured applications span MEMS/NEMS, MOEMS, bioelectronics, displays, photonics, metamaterials, AR/VR, and micro/nanofluidics. Diverse approaches including maskless techniques, roll-to-roll processes, 3D printing, DNA-based and colloidal self-assembly, and additive manufacturing are welcomed. Contributions are also sought on hybrid methodologies integrating top-down lithographic and bottom-up patterning processes such as directed self-assembly (DSA), self-aligned pitch division, tone-reversals, area-selective or templated depositions, and novel bio-inspired assembly of functional nanomaterials.

APPLICATION AREAS FOR NOVEL PATTERNING TECHNOLOGIES

- functional nanopatterning materials and emerging IoT applications
- novel patterning for leading edge semiconductor nodes and beyond
- MEMS/NEMS, MOEMS, and microsystems
- metasurfaces and metamaterials
- photonic and/or phononic crystals
- micro/nanofluidics, lab on a chip or other bio-applications
- digital micro-mirror arrays
- multi-beam writing of masks and master templates
- semiconductor wafer-level packaging and fan-out
- bioelectronics and genomics/proteomics
- photovoltaics and related energy applications
- large-area display/flat-panel displays
- roll-to-roll/web format device manufacturing
- micro LED array fabrication
- nanopatterned sensors, waveguides, antennas
- building blocks for defect-tolerant computing
- smart resists and self-healing materials
- tools/materials to improve existing scanner performance
- quantum computing devices and qubit-technologies
- heterogeneous and monolithic 3D integration and materials
- neuromorphic and emerging memory patterning
- atomistic nanoelectronic devices
- AI-driven or autonomous manufacturing
- sustainable patterning technologies

Novel Patterning Technologies 2025 (AL104)
continued

TECHNOLOGY AREAS FOR NOVEL PATTERNING APPLICATIONS

DIRECT WRITE OR MASKLESS LITHOGRAPHY AND PATTERNING TECHNOLOGIES
- electron or ion charged-particle beams
- optical beams
- STED, multi-color/multi-photon direct write
- resistless e-beam or ion beam direct patterning
- beam-directed nucleation, ion-beam deposition
- material ablation or material transformation reactions
- ink-jet
- scanning probe lithography, dip-pen printing, tip-based patterning
- interference, plasmonic or nearfield/evanescent wave lithography
- micromirror optical lithography
- 3D metal or ceramic sintering

PROCESS BASED LITHOGRAPHY AND PATTERNING
- directed self-assembly
- nanoimprint lithography
- selective deposition
- self-aligned or pitch division process integration techniques
- colloidal self-assembly and DNA patterning
- 3D patterning
- mechanical patterning
- additive manufacturing

In the spirit of facilitating exchange of knowledge, we strongly encourage contributions that provide a background to the technology, details on latest results and a clear indication of the limitations/opportunities for future development.

NOVEL PATTERNING TECHNOLOGIES STUDENT AWARD 2025

Recognizing the invaluable contributions made by students to our patterning community, the conference proudly presents a "Best Student Paper Award," generously sponsored by Meta. Eligible candidates must be enrolled as students in a relevant STEM field at the time of presentation and submit a proceedings manuscript (2-page minimum) by February 5, 2025. Student presentations will be evaluated on the basis of their technical merit, novelty, presentation quality and communication skills. The award will include a certificate and a monetary gift.

Students are also encouraged to apply for travel grants to attend the conference and for the Nick Cobb Memorial Scholarship.

Submit your abstract today: **www.spie.org/alcall**

Advances in Patterning Materials and Processes XLII (AL105)

Conference Chair: **Gilles R. Amblard,** SAMSUNG Austin Semiconductor LLC (United States)

Conference Co-Chair: **Ryan Callahan,** FUJIFILM Electronic Materials U.S.A., Inc. (United States)

Program Committee: **Ramakrishnan Ayothi,** JSR Micro, Inc. (United States); **Luisa D. Bozano,** Applied Materials, Inc. (United States); **Robert L. Brainard,** SUNY Polytechnic Institute (United States); **Ralph R. Dammel,** EMD Electronics (United States); **Anuja De Silva,** Lam Research Corp. (United States); **Danilo De Simone,** imec (Belgium); **Roel Gronheid,** KLA Corp. (Belgium); **Jara Garcia-Santaclara,** ASML Netherlands B.V. (Netherlands); **Douglas Guerrero,** Brewer Science, Inc. (United States); **Masahiko Harumoto,** SCREEN Semiconductor Solutions Co., Ltd. (Japan); **Clifford L. Henderson,** The Univ. of Alabama (United States); **Christoph K. Hohle,** Fraunhofer-Institut für Photonische Mikrosysteme IPMS (Germany); **Xisen Hou,** DuPont Electronics & Imaging (United States); **Dario L. Goldfarb,** IBM Thomas J. Watson Research Ctr. (United States); **Scott W. Jessen,** Texas Instruments Inc. (United States); **Jing Jiang,** Applied Materials, Inc. (United States); **Yoshio Kawai,** Shin-Etsu Chemical Co., Ltd. (Japan); **Tetsu Kohyama,** Nihon Entegris G.K. (Japan); **Marie E. Krysak,** Intel Corp. (United States); **Qinghuang Lin,** Lam Research Corp. (United States); **Nobuyuki N. Matsuzawa,** Panasonic Corp. (Japan); **Warren Montgomery,** EMD Electronics (United States); **Tomohiro Oikawa,** Tokyo Ohka Kogyo America, Inc. (United States); **Mark H. Somervell,** Tokyo Electron America, Inc. (United States); **Ankit Vora,** Meta (United States)

EXTENDED ABSTRACT REQUEST

An optional PDF file is requested in step 7 of the abstract submission process:
- 2-page maximum extended abstract. The extended abstract must be submitted as a separate PDF document limited to two pages, including tables and figures. Include author names and affiliations; text; any figures; tables, or images; and sufficient data for committee review.

Extended abstracts will be used only for the purpose of review and will not be published.

The Advances in Patterning Materials and Processes conference is the leading forum for scientists and engineers from institutes, material as well as equipment vendors, and end-users around the world to present and discuss research on the chemistry, physics, and performance of photoresists and patterning materials and processes. Evolutionary and ultimately revolutionary innovations will continue to be required in materials and patterning processes in order to achieve the combination of resolution, edge roughness, and sensitivity required for future technology nodes and innovative emerging technologies.

This conference welcomes submissions of original papers that emphasize recent advances in high-performance patterning processes and materials and their integration in established, maturing, emerging, and new lithographic technologies including patterning for augmented reality (AR) and virtual reality (VR) applications. Original technical papers are solicited, but not limited to the following topics:

PATTERNING MATERIALS, PROCESSES, AND APPLICATIONS
- Materials for EUV and high NA EUV lithography
- Materials for other wavelengths: electron beam or other maskless lithography, ArF dry and wet, KrF, i-line, and g-line
- Novel development techniques: positive and negative tone (PTD, NTD) photoresists and developers, solvent, aqueous, or dry development processes
- Multi-layer patterning materials: underlayers, Bottom Anti-Reflective coatings, and materials for planarization, pattern transfer, and process enhancement
- Selective deposition and surface modification of organic and inorganic materials: chemistry, processing, and materials science, bottom-up approaches
- Directed self-assembling materials (DSA): chemistry and materials science, processing, and ancillary materials
- Materials and processes used in vertical integration of novel devices, stacked structures, nanosheets, nanotubes, solvent based or dry processes
- Materials for packaging and SOC/SIP integration
- Materials for patterning and optical control of AR/VR applications
- Sustainable PFAS/PFOS free materials, roadmap for compliance with regulatory legislation and plans for phasing out PFAS/PFOS containing materials by the suppliers community
- Patternable dielectric materials

PROCESSING AND PROCESS CONTROL
- Single and multiple patterning
- Patterns smoothing, rectification, pattern collapse prevention, trim and shrink, and tone inversion
- Applied processing, including filtration, defect control, and pattern collapse mitigation
- Materials challenges related to etch, process control, and metrology
- New processing techniques and applications, especially self-aligned and additive strategies
- Innovative patterning materials for advanced integration schemes
- Sustainable and environmentally acceptable processes, low energy, solvent, or water consumption

Advances in Patterning Materials and Processes XLII (AL105) continued

SIMULATION AND MODELING

- Resist fundamentals and assessment of patterning and materials scaling limits
- Variability, stochastics, and defectivity
- Design for or simulation of new processes and applications
- Artificial Intelligence and Machine Learning approaches to materials design, characterization, patterning, and process control.

Consistent with the conference's charter and goals, authors are required to provide a description of chemical and physical principles as well as sufficient chemical structural detail in the presented work. Submissions which do not reveal sufficient chemical details to add value to the readers or are principally of a commercial nature may not be accepted for presentation and publication.

AWARDS

Each year the SPIE Patterning Materials and Processes Conference recognizes the outstanding oral, poster, and student submissions from the prior year's conference via three distinguished awards:

C. GRANT WILLSON BEST PAPER AWARD IN PATTERNING MATERIALS AND PROCESSES

The C. Grant Willson Best Paper Award in Patterning Materials and Processes recognizes the best oral paper presented at the previous year. Candidate papers are nominated and selected by the SPIE Patterning Materials conference committee. Judging criteria include the technical originality, completeness, relevance, quality of oral presentation, and quality of proceedings manuscript. Invited keynote talks are not eligible. The award consists of a certificate and a cash honorarium of $1,000 USD.

AWARD SPONSORED BY

JEFFREY BYERS BEST POSTER AWARD IN PATTERNING MATERIALS AND PROCESSES

The Jeffrey Byers Best Poster Award in Patterning Materials and Processes recognizes the best poster presented at the previous year. Candidate posters are nominated and selected by the SPIE Patterning Materials conference committee. Judging criteria include the technical originality, completeness, relevance, quality of poster presentation, and quality of proceedings manuscript. The award consists of a certificate and a cash honorarium of $1000 USD.

AWARD SPONSORED BY

TEL

HIROSHI ITO STUDENT AWARD IN PATTERNING MATERIALS AND PROCESSES

The Hiroshi Ito Student Award in Patterning Materials and Processes recognizes the best student paper presented at the previous year. Candidate papers are nominated and selected by the SPIE Patterning Materials conference committee. To be eligible, the primary and presenting author must be a student or post-doc at the time of the conference. Judging criteria include the technical originality, completeness, relevance, quality of presentation, and quality of proceedings manuscript. Both oral and poster submissions are eligible; however, the award will not be given to a submission that is a concurrent winner of the Willson or Byers Awards. The award consists of a certificate and a cash honorarium of $1,000 USD.

AWARD SPONSORED BY

Students are encouraged to apply for travel grants to attend the conference and for the Nick Cobb Memorial Scholarship.

Advanced Etch Technology and Process Integration for Nanopatterning XIV (AL106)

Conference Chair: **Nihar Mohanty,** Meta (United States)

Conference Co-Chair: **Efrain Altamirano-Sánchez,** imec (Belgium)

Program Committee: **Aleksandar Aleksov,** Intel Corp. (United States); **John C. Arnold,** IBM Thomas J. Watson Research Ctr. (United States); **Keun Hee Bai,** SAMSUNG Electronics Co., Ltd. (Republic of Korea); **Julie Bannister,** Tokyo Electron America, Inc. (United States); **Robert L. Bruce,** IBM Thomas J. Watson Research Ctr. (United States); **Thierry Chevolleau,** MINATEC (France); **Sebastian U. Engelmann,** IBM Thomas J. Watson Research Ctr. (United States); **John Hoang,** Lam Research Corp. (United States); **Catherine B. Labelle,** Intel Corp. (United States); **Qinghuang Lin,** Lam Research Corp. (United States); **Jake O'Gorman,** Hitachi High-Tech America, Inc. (United States); **Prem Kumar Panneerchelvam,** KLA Texas (United States); **Erwine Pargon,** Lab. des Technologies de la Microélectronique (France); **Angélique Raley,** TEL Technology Ctr., America, LLC (United States); **Ricardo Ruiz,** Lawrence Berkeley National Lab. (United States); **Gurpreet Singh,** Intel Corp. (United States); **Yuyang Sun,** Siemens EDA (United States); **Richard S. Wise,** Lam Research Corp. (United States); **Ying Zhang,** NAURA (United States)

EXTENDED ABSTRACT REQUEST

An optional PDF file is requested in step 7 of the abstract submission process:

- 2-page maximum extended abstract. The extended abstract must be submitted as a separate PDF document limited to two pages, including tables and figures. Include author names and affiliations; text; any figures; tables, or images; and sufficient data for committee review.

Extended abstracts will be used only for the purpose of review and will not be published.

The revolution in microelectronics over the last fifty years, driven by Moore's Law, has been propelled by continuous acceleration in the dimensional scaling of logic and memory semiconductor devices. Dramatic innovations in optical and now extreme ultraviolet lithography, in conjunction with novel process integration strategies, have been the driving force behind much of the success of dimensional scaling. Plasma-based pattern transfer innovations have formed a major backbone for those integration strategies that in collaboration with wavelength and numerical aperture scaling have avoided the physical limits as defined by the Rayleigh criterion. This dimensional scaling has defined a patterning era, leveraging innovative plasma processing techniques and novel process integration to significantly extend achievable pattern design, dimension, and fidelity. Novel integration strategies elevate the basic elements to the next level by enabling more complex structures with high fidelity, not only for traditional semiconductor logic and memory but also for advanced photonics, 3D integration, packaging, and more.

This new paradigm presents new opportunities for novel plasma-based processes (etch and deposition), as well as for gas and liquid phase isotropic processes, which are crucial to a comprehensive patterning strategy. The increasingly complex interdependence of lithography, material deposition, and photoresist, combined with process technologies such as plasma etch, gas etch, and wet etch, has created new opportunities in materials, integration, and the co-optimization of patterning and process control. Historically distinct from optical imaging, the emerging role of these new patterning techniques and process integration in defining critical on-device features has driven a need for more intelligent process control and automated development

Original and overview technical papers are solicited on, but not limited to, the following topics:

- Novel developments in plasma-based patterning techniques: EUV-based patterning, self-aligned spacer techniques (SAxP and mandrel/spacer design), optical lithography patterning, complementary patterning and optical/EUV tradeoffs, self-aligned structures, on product overlay, edge placement error mitigation strategies, and cost modeling of the proposed patterning schemes
- Novel discoveries of plasma-material interactions: plasma-photoresist interactions, LER/LWR/stochastics mitigation, MOL/BEOL (low-k) material interactions, novel substrate material handling (SiGe, III-V, C, nonvolatile memory) etc.
- Novel etch challenges for AI architectures, 3D memory and logic architectures
- Defect reduction or yield enhancement techniques by dry or wet process solutions
- New etch methodologies and their application to patterning processes, e.g.: cryogenic etching, atomic layer etching (ALE), low Te processing, high aspect ratio pattern definition, selective deposition, gas phase isotropic etch and wet etch processing.
- Patterning control through advanced process solutions: in-situ process control, process simulations, etch-aware OPC, edge place error (EPE) etc.
- Plasma process & equipment modeling and simulation to accelerate time-to-solution for equipment and process recipe development through mechanistic understanding of processes and faster and wider exploration of process recipe space.
- AI machine-learning-based methodologies for process or equipment development

Advanced Etch Technology and Process Integration for Nanopatterning XIV (AL106)

continued

- Novel integration strategies for pattern fidelity improvement, new design enablement, etc.
- Novel holistic (litho, etch, and deposition) patterning solutions for logic and memory applications
- Advanced integration & patterning solutions for emerging product applications including but not limited to: AI chipset architectures, AR/VR, neuromorphic computing, quantum computing, power semiconductors (GaN, others), IoT devices, MEMS, MOEMS, other “more than Moore devices” and derivative technologies (RF, analog or mixed signal)
- Novel packaging integration & patterning solutions for advanced node logic & memory in the AI era (Eg. TSV etch, Heterogenous-wafer alignment)
- Advances in etch or patterning technology that enable sustainability goals for the semiconductor industry.

Abstracts with a preview of results and conclusions supported by technical data are favored for oral presentation.

Sessions for 2025

- Materials and Etch Integration
- Computational Patterning, Patterning Process Control and Plasma process modeling & simulation
- EUV Patterning and Etch
- Advanced Patterning Integration including 3D monolithic integration (Eg. CFET, Backside power management, etc)
- Novel Atomic Scale Processes
- Advanced Packaging & Emerging 2.5D/3D Heterogeneous integration
- Optical & Photonic Patterning and Integration Applications (AI architectures, Quantum computing, AR/VR, MicroDisplays, Metalenses, Sensing, Imaging, etc)
- Sustainability in Etch, Patterning and Process Integration

THE ADVANCED ETCH TECHNOLOGY AND PROCESS INTEGRATION BEST STUDENT PAPER AWARD

Continuing from last year, the Advanced Etch Technology and Process Integration conference will offer a ***Best Student Paper Award*** sponsored by Meta. All student paper submissions automatically qualify for consideration by the committee. The award will recognize the paper with the most significant contribution and innovation for solving advanced patterning challenges and the quality of the oral presentation/ poster presentation. After the paper presentation, the committee will vote for the best paper, and the award winner is notified by the conference chairs and SPIE. The award will include a certificate and monetary gift.

Students are also encouraged to apply for travel grants to attend the conference and for the Nick Cobb Memorial Scholarship.

Submit your abstract today: **www.spie.org/alcall**

Student opportunities at Advanced Lithography + Patterning

STUDENTS: LEARN HOW TO ATTEND FOR FREE

US students can receive up to $500 and international students can receive up to $1,000 to cover travel costs. Travel costs that can be reimbursed include air fare, gas, and/or trains, and also lodging, such as hotel or Airbnb. Students will also be able to choose one short course they'd like to attend onsite, and the registration will be covered by the grant.

Deadline to apply for grant: **21 November 2024**

Learn more about grants sponsored by companies and the application process at: https://spie.org/studentgrant

NICK COBB MEMORIAL SCHOLARSHIP

The US $10,000 Nick Cobb Memorial Scholarship is awarded to an outstanding graduate student studying advanced lithography or a related field. The funding can be used to support tuition and fees, textbooks, supplies and equipment required for courses of instruction, and a computer or computer upgrade.

The scholarship is jointly funded by Siemens EDA and SPIE. In addition to the $10,000 scholarship, Siemens EDA provides the recipient travel support to SPIE Advanced Lithography + Patterning to receive the award.

The scholarship honors the memory of Nick Cobb, an SPIE Senior Member and Chief Engineer at Mentor Graphics, now Siemens EDA, and his groundbreaking contributions enabling optical and process proximity correction for IC manufacturing.

The 2024 application is open. **Apply by 6 October 2024.**

Present your research at SPIE Advanced Lithography + Patterning

Follow the instructions below to develop a successful abstract for submission to a conference and review policies for publication in the Proceedings of SPIE in the SPIE Digital Library. Submissions subject to chair approval.

Important dates

Abstracts due	11 September 2024
Registration opens	November 2024
Author notified and program posts online	18 November 2024
Student Grant applications due	21 November 2024
Submission system opens for manuscripts and poster PDFs*	23 December 2024
Poster PDFs due for spie.org preview and publication	29 January 2025
Advance upload deadline for oral presentation slides**	21 February 2025
Manuscripts due	12 February 2025

*Contact author or speaker must register prior to uploading
**After this date slides must be uploaded onsite at Speaker Check-In

What you will need to submit

- Presentation title
- Author(s) information
- Speaker biography (1000-character max including spaces)
- Abstract for technical review (200-300 words; text only)
- Summary of abstract for display in the program (50-150 words; text only)
- Extended abstract PDF document limited to two pages maximum, including tables and figures. Include author names and affiliations; text; any figures; tables, or images; and sufficient data for committee review
- Keywords used in search for your paper (optional)

Note: Only original material should be submitted. Commercial papers, papers with no new research/development content, and papers with proprietary restrictions will not be accepted for presentation.

How to submit your abstract

- Visit the conference page: www.spie.org/ALcall
- You may submit more than one abstract, but submit each abstract only once
- Submit by clicking the "Submit an Abstract" button on the conference page
- Sign in to your SPIE account, or create an account if you do not already have one
- Follow the steps in the submission wizard until the submission process is completed
- If your submission is related to an application track below, indicate the appropriate track when prompted during the submission process

Application tracks

- An application track is a grouping of presentations on a topic of interest across all conferences. During submission of the abstract, the submitting author should select an application track if it is relevant to their research.
- **AI/ML:** Papers that highlight the use of artificial intelligence, machine learning, and deep learning to create and implement intelligent systems across multiple sectors, technologies, and applications
- **Sustainability:** Papers that highlight the use of optics and photonics for renewable energy, natural resource management, sustainable manufacturing, and greenhouse gas mitigation in support of the UN Sustainable Development Goals
- **Stochastics:** Papers related to Line Edge Roughness (LER), Line Width Roughness (LWR), photon and secondary electron stochastics, chemical and process nonuniformity
- **Advanced Packaging:** The interconnection of multiple integrated devices, including electronic, photonic, and/or MEMS, to be packaged as a single component. Advanced packaging achieves performance gains through the integration of several devices in one package, driving heterogenous integration and chiplet architectures.
- **EPE/Overlay:** Papers related to overlay, CD, and Edge Placement Error (EPE); characterization and metrology, root cause analysis, and process improvements.

Submission agreement

All presenting authors, including keynote, invited, oral, and poster presenters, agree to the following conditions by submitting an abstract:

- Register and pay the conference registration fee
- Agree to receive email messaging for the conference series
- Oral presenters: agree to recording and publication of your onsite presentation (slides synched with voice) in the Proceedings of SPIE in the SPIE Digital Library
- Poster presenters: one person may not present more than two posters in a poster session; submit a poster PDF for preview in the online program (web and app) and for publication in the Proceedings of SPIE in the SPIE Digital Library
- Submit a manuscript by the advertised due date for publication in the Proceedings of SPIE in the SPIE Digital Library
- Obtain funding for registration fees, travel, and accommodations
- Attend the meeting
- Present at the scheduled time

Review and program placement

- To ensure a high-quality conference, all submissions will be assessed by the conference chair/editor for technical merit and suitability of content
- Conference chairs/editors and/or SPIE staff reserve the right to reject for presentation any paper that does not meet content or presentation expectations
- Final placement in an oral or poster session is subject to chair discretion

Publication of Proceedings in the SPIE Digital Library

Increase your professional visibility and publish in the world's largest collection of optics and photonics research. Your peers access approximately 18 million papers, presentations, and posters from the SPIE Digital Library each year.

- Only manuscripts, presentations, and posters presented at the conference and received according to publication guidelines and due dates will be published in the Proceedings of SPIE in the SPIE Digital Library
- Manuscripts, presentations, and posters will be officially published after the event in the SPIE Digital Library
- Conference chairs/editors or SPIE staff may require revision before approving publication and reserve the right to reject for publication any manuscript or presentation that does not meet acceptable standards for a scientific publication
- Conference chair/editor and/or SPIE staff decision to accept or reject a manuscript, presentation, or poster for publication is final
- Authors must be authorized to provide a suitable publication license to SPIE; authors retain copyright of all scientific material
- SPIE retains rights to distribute and market the official SPIE recording of the presentation and/or submitted poster
- SPIE partners with relevant scientific databases and indexes to enable researchers to easily find papers published in the Proceedings of SPIE. The databases that abstract and index these papers include Astrophysical Data System (ADS), Ei Compendex, CrossRef, Google Scholar, Inspec, Scopus, and Web of Science
- More publication information available on the SPIE Digital Library

Contact information

QUESTIONS?

Contact the coordinator listed in your spie.org account.

For questions about your presentation, submitting an abstract or the meeting, contact your conference program coordinator.

For questions about publication or the SPIE Digital Library, contact your proceedings coordinator.

SPIE. DIGITAL LIBRARY

SPIE WILL PUBLISH YOUR RESEARCH GLOBALLY

www.SPIEDigitalLibrary.org

Your work will live far beyond the conference room—all proceedings from this meeting will be published in the SPIE Digital Library. Promote yourself, your ideas, and your organization to millions of key researchers from around the world through this web-based repository of the latest technical information.

SPIE.

SPIE is the international society for optics and photonics. We bring together engineers, scientists, students, and industry leaders, strengthening the global optics and photonics community through conferences, publications, and professional development. Inspired by the transformative power of photonics to enhance life around the globe, over the past five years SPIE has contributed more than $24 million to the international optics community.

SPIE is a registered trademark of the Society of Photo-Optical Instrumentation Engineers. All rights reserved.

SPIE International Headquarters
PO Box 10
Bellingham, WA 98227-0010 USA
Tel: +1 360 676 3290 / Fax: +1 360 647 1445
customerservice@spie.org / www.SPIE.org

SPIE Europe Office
2 Alexandra Gate
Ffordd Pengam, Cardiff, CF24 2SA UK
Tel: +44 29 2089 4747
info@spieeurope.org / www.SPIE.org

SPIE Journal of Optical Microsystems

The *Journal of Optical Microsystems* publishes cutting-edge research in all aspects of optical and photonic microsystems, from materials and fabrication of micro-optical and photonic components, through assembly and packaging, to systems and applications.

About the Editor

Hans Zappe is the Gisela and Erwin Sick Professor of Micro-Optics at the University of Freiburg in Germany.

SPIE.

www.spie.org/JMI

As a center of innovation, San Jose welcomes you

San Jose, California in the U.S. boasts the largest concentration of technology expertise in the world. San Jose also leads the nation in patent generation. The city has 25 companies with 1,000 employees or more, including the headquarters of Adobe Systems, BEA Systems, Cisco, Xilinx, Lam Research, and eBay, as well as major facilities for Flextronics, Hewlett-Packard, IBM, Hitachi, Agilent Technologies, and Lockheed Martin.

VENUE

SPIE Advanced Lithography + Patterning

San Jose McEnery Convention Center

150 West San Carlos Street

San Jose, CA 95110

Additional event space and hotel rooms will be hosted at San Jose Marriott, which is located nearby.The perfect setting for business or pleasure, the conference hotel has been a landmark destination in Mission Valley, San Diego for close to 60 years and offers a premier location near many popular San Diego attractions and activities. The newly remodeled Town and Country is a modern expression of the 1960s Southern California vibe, relaxed, playful, and where everyone feels welcome.

HOTEL INFORMATION COMING SOON

Hotel options and reservation details will be available at a later date. Booking through SPIE provides the best offers.

REGISTRATION

Registration will open in November

We look forward to seeing you in at SPIE Advanced Lithography + Patterning 2025. Keep up to date on information and registration details. Stay connected and sign up to be notified when registration opens.

TRAVEL TO SAN JOSE

Information will be provided for:

airport

shuttle service

public transit services

car rental

driving directions and parking

tourist attractions

Check website for updates: www.spie.org/al24call

Submit your abstract today: **www.spie.org/al24call**

SPIE. DIGITAL LIBRARY

Access the 2024 research and recordings

SPIE Advanced Lithography + Patterning 2024 conference proceedings papers and presentation recordings are published in the SPIE Digital Library. Review the research that has been shared as you prepare to submit your work for 2025.

www.SPIEDigitalLibrary.org